

PTO/SB/08A (07-05)

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## **INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

*(Use as many sheets as necessary)*

Sheet 1 of 2

Complete if Known	
Application Number	10/849,692
Filing Date	05/19/2004
First Named Inventor	Jared L. Zerbe
Art Unit	2661
Examiner Name	Unknown
Attorney Docket Number	RA328.P.US

**U. S. PATENT DOCUMENTS**

## **FOREIGN PATENT DOCUMENTS**

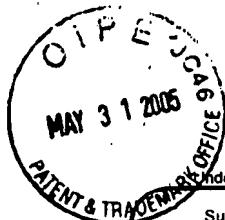
FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T
		Country Code <sup>2</sup> -Number <sup>4</sup> -Kind Code <sup>3</sup> (if known)				
/DC/	4	EP 1 424 871 A2	02.06.2004	Alcatel Canada Inc.		
↓	5	WO 00/65791	02.11.2000	Greigh, John L.		
↓	6	EP 0 886 407 A2	23.12.1998	Hewlett-Packard Company		

Examiner Signature:	/Dady Chery/	Date Considered	08/09/2007
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*(Use as many sheets as necessary)*

Sheet

of 1

PTO/SB/08A (08-03)

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U.S. Department of Commerce, Patent and Trademark Office		Serial No.: Unknown
		Filing Date: May 19, 2004
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Inventor: Jared L. Zerbe
"Crosstalk Minimization in Serial Link Systems"		Group Art Unit: Unknown
Express Mail No. ER 265640992 US		Examiner Name: Unknown
		Attorney Docket No.: RA328.P.US

U.S. Patent and U.S. Patent Publication Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
/DC/	A	6,396,887 B1	05/28/02	Ware et al.	375	354	
	B	6,366,991 B1	04/02/02	Manning	711	167	
	C	5,509,038	04/16/96	Wicki	375	371	
	D	6,661,863 B1	12/09/03	Toosky	375	376	
	E	6,504,438 B1	01/07/03	Chang et al.	331	17	
	F	US 2003/ 0053489 A1	03/20/03	Zerbe et al.	370	503	
	G	US 2003/ 0099190 A1	05/29/03	Zerbe	370	201	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

H	JOHNSON, HOWARD DR., "Mitigating Crosstalk." High-Speed Digital Design - online newsletter - Vol. 6, Issue 01. January 20, 2003. Pages 1-3.
I	"Shift Register Counters." Downloaded from <a href="http://www.eelab.usyd.edu.au/digital tutorial/part/2/registro07.htm">http://www.eelab.usyd.edu.au/digital tutorial/part/2/registro07.htm</a> . 09/17/02. 2 pages.
J	STOJANOVIC, VLADIMIR et al., "Modeling and Analysis of High-Speed Links." Research supported by the MARCO Interconnect Focus Center and Rambus, Inc. September 2003. 8 pages.
K	SIDIROPOULOS, STEFANOS et al., "Adaptive Bandwidth DLLs and PLLs Using Regulated Supply CMOS Buffers." 2000 Symposium of VLSI Circuits Digest of Technical Papers. 4 pages.
L	SIDIROPOULOS, STEFANOS et al., "A Semidigital Dual Delay-Locked Loop." IEEE Journal of Solid-State Circuits, Vol. 32, No.11, November 1997. Pages 1683-1692.
M	STOJANOVIC, VLADIMIR et al., "Adaptive Equalization and Data Recovery in a Dual-Model (PAM 2/4) Serial Link Transceiver." Rambus, Inc. Department of Electrical Engineering, Stanford University. January 2004. 4 pages.

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## U.S. Patent and U.S. Patent Publication Documents

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	N						
	O						
	P						
	Q						
	R						
	S						

## OTHER ART. (Including Author, Title, Date, Pertinent Pages, Etc.)

/DC/	T	CHANG, KUN-YUNG KEN et al., "A 0.4-4Gb/s CMOS Quad Transceiver Cell Using On-Chip Regulated Dual-Loop PLLs." Rambus Inc., Los Altos, CA; T-RAM, San Jose, CA; Aeluros Inc, Mountain View, CA. May 2003. 4 pages.
	U	FARJAD-RAD, RAMIN, "A 0.4-μm CMOS 10-Gb/s 4-PAM Pre-Emphasis Serial Link Transmitter." Center for Integrated Systems, Stanford University, Stanford, CA. May 1999. 2 pages.
	V	ZAND, BAHRAM et al., "High-Speed CMOS Analog Viterbi Detector for 4-PAM Partial Response Signalling." University of Toronto, Toronto, Canada. July 2002. 4 pages.
	W	ZERBE, J. et al., "Equalization and Clock Recovery for a 2.5 - 10 Gbs 2-PAM/4-PAM Backplane Transceiver Cell." Presented at ISSCC 2003, paper 4.6 2 pages.
↓	X	ZERBE, JARED L. et al., "Equalization and Clock Recovery for a 2.5-10-Gb/s 2-PAM/4-PAM Backplane Transceiver Cell." IEEE Journal of Solid-State Circuits, Vol. 38, No. 12, December 2003. Pages 2121-2130.
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